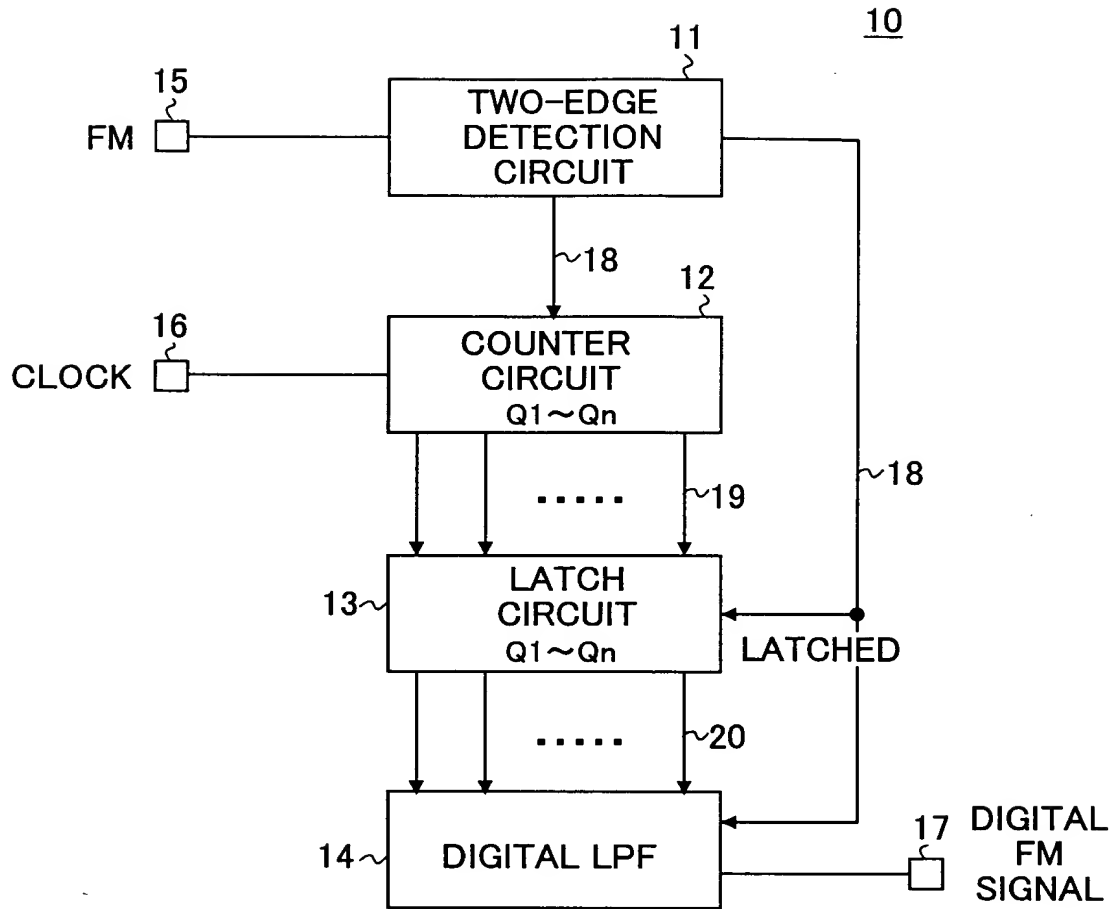


FIG.1 PRIOR ART



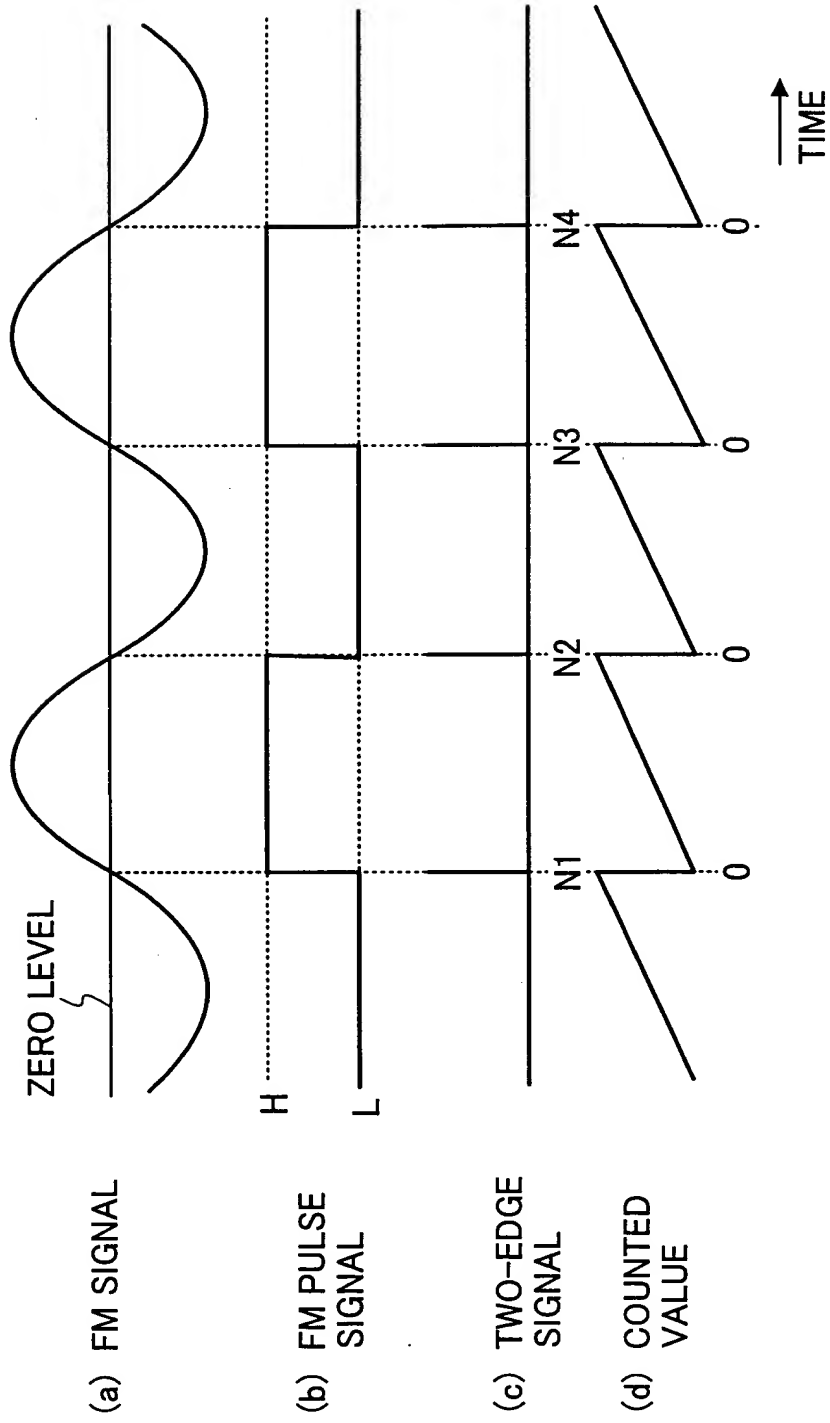


FIG.2
PRIOR
ART

097440666.034901
T06T00 99907260

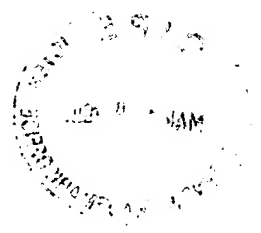
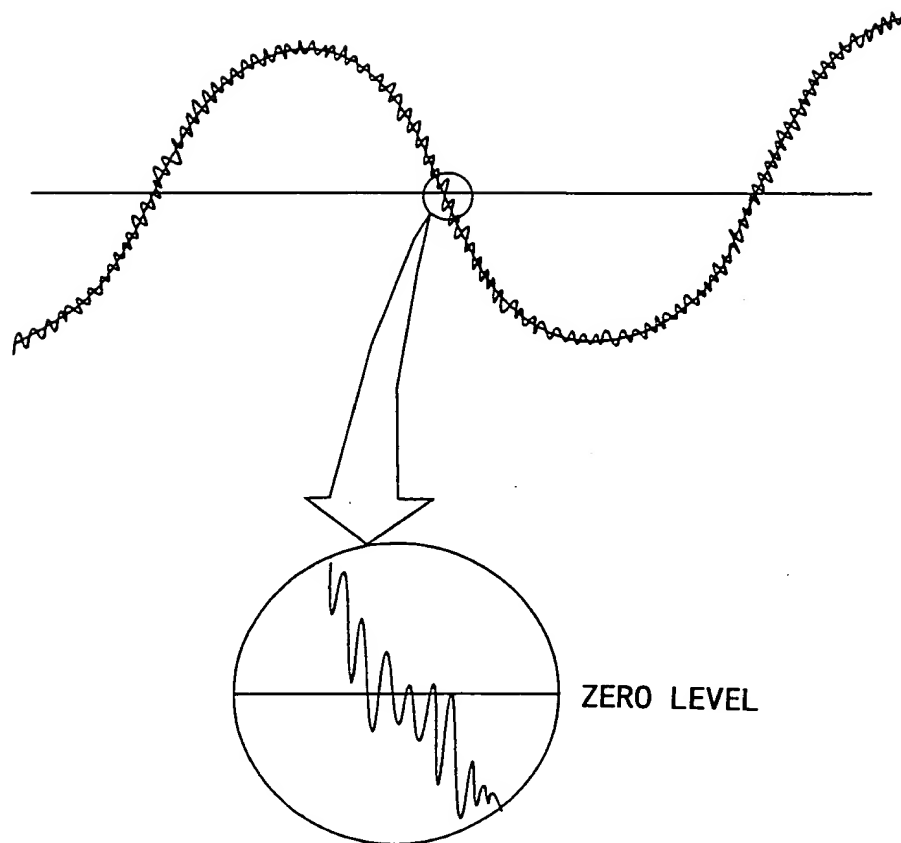


FIG. 3 PRIOR ART



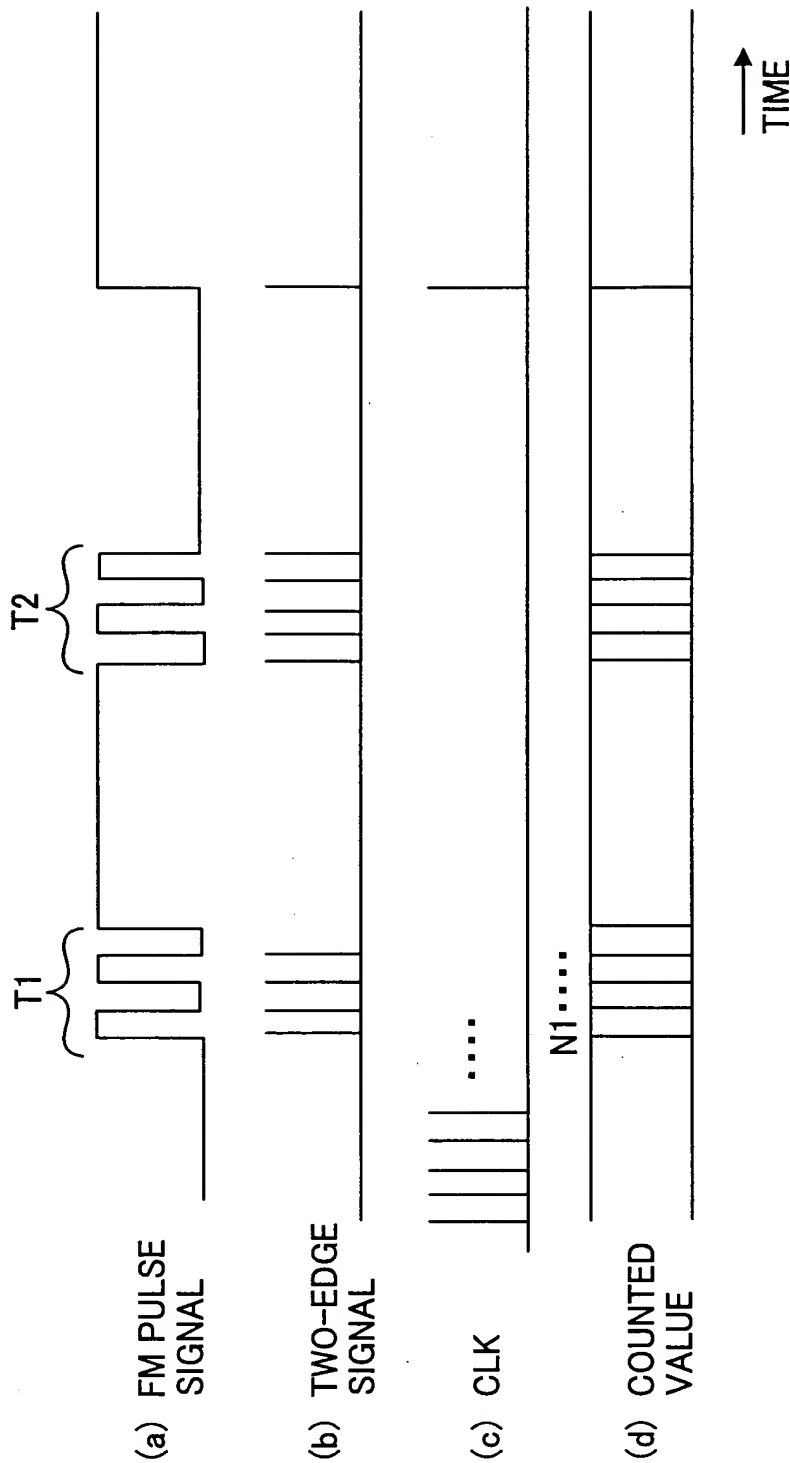


FIG.4
PRIOR
ART

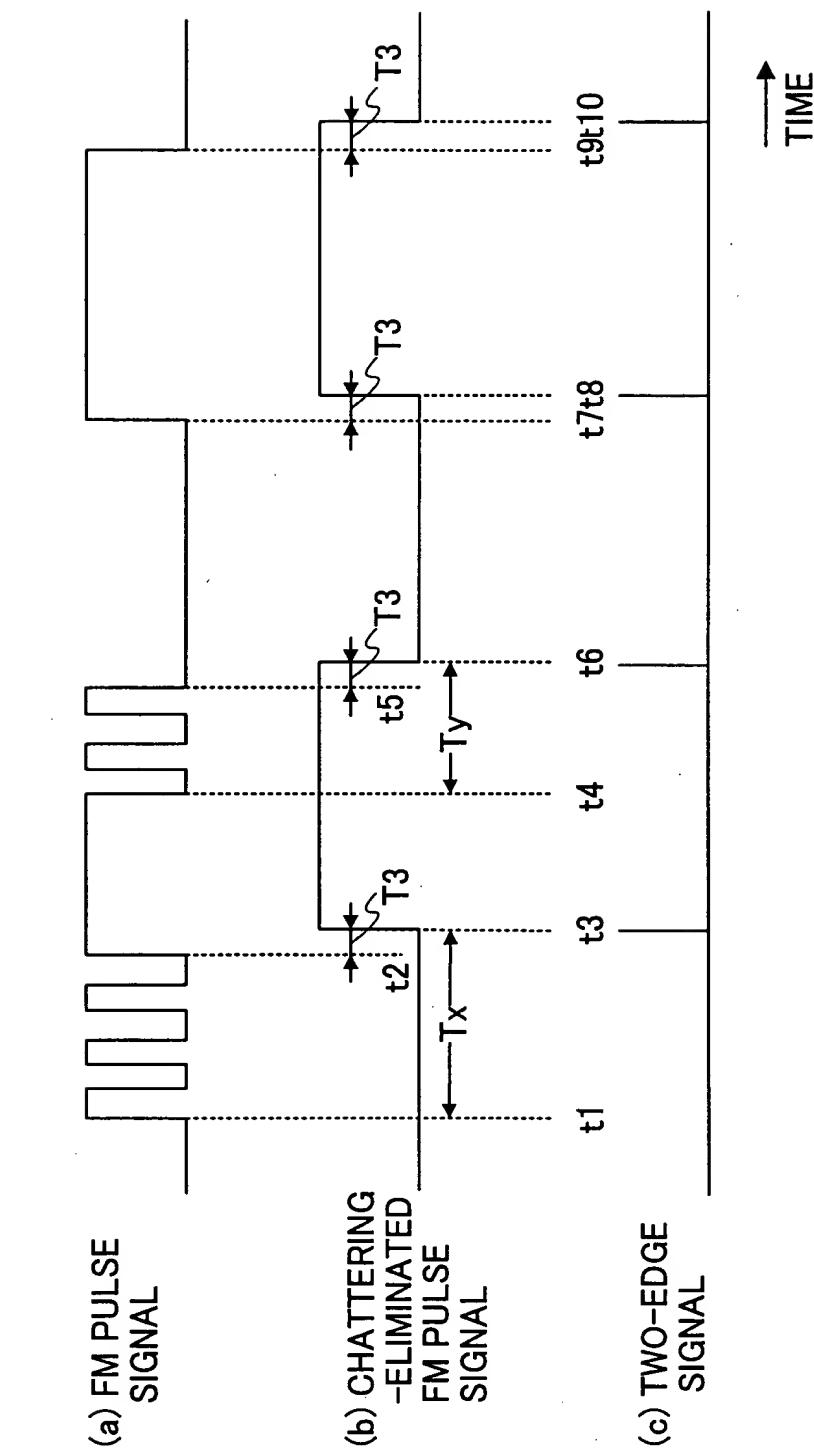


FIG.5
PRIOR
ART

FIG.6

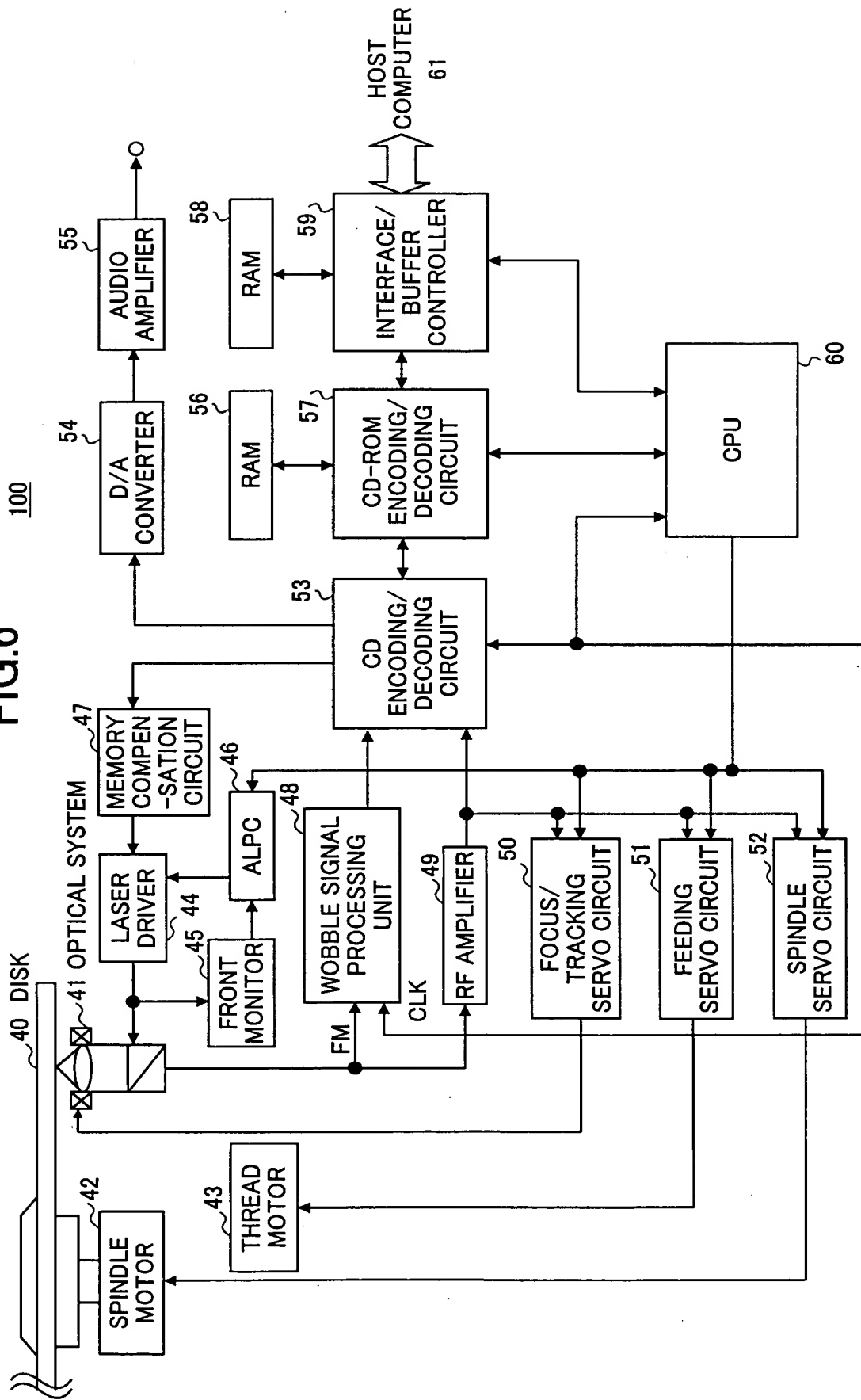
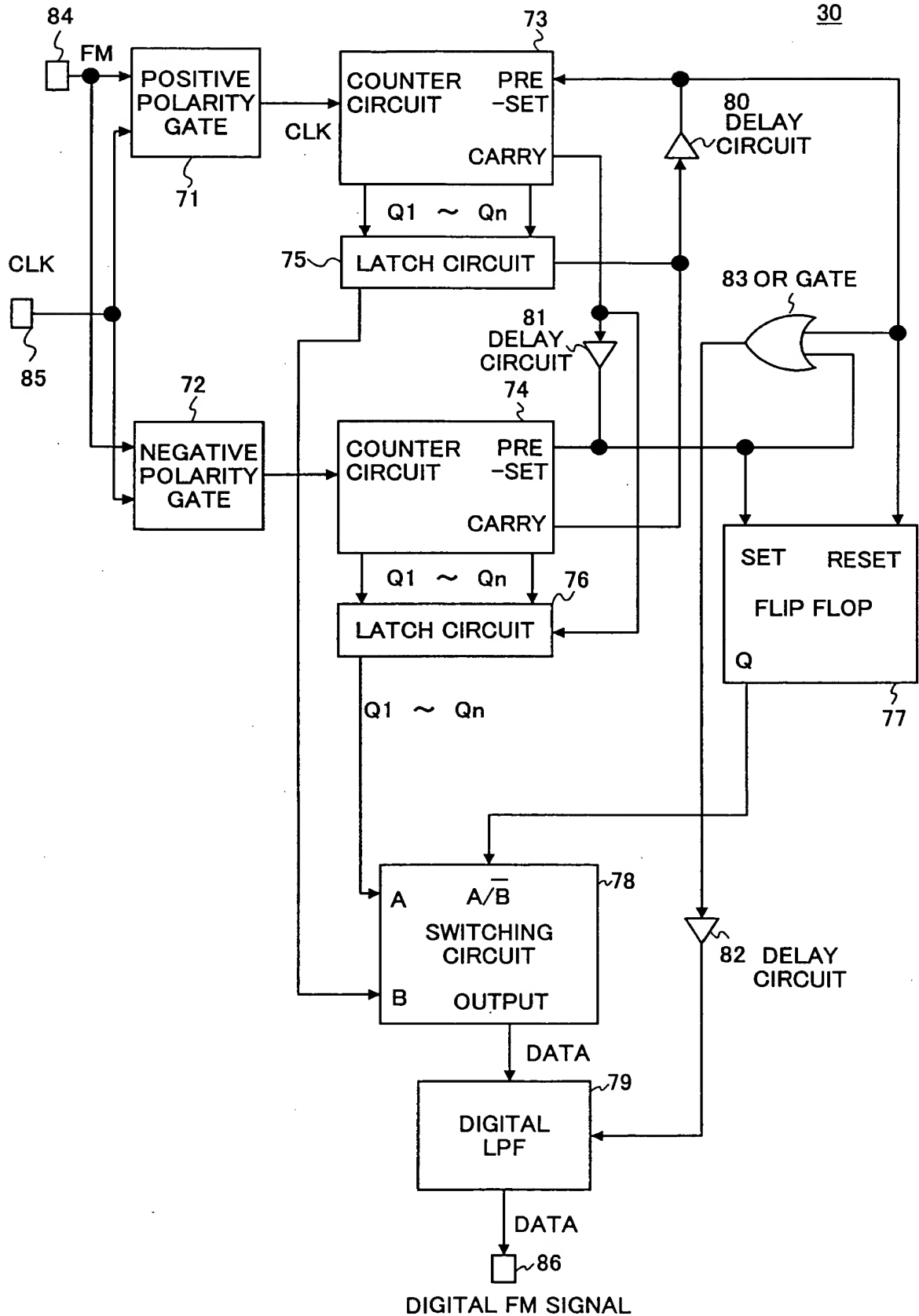


FIG.7



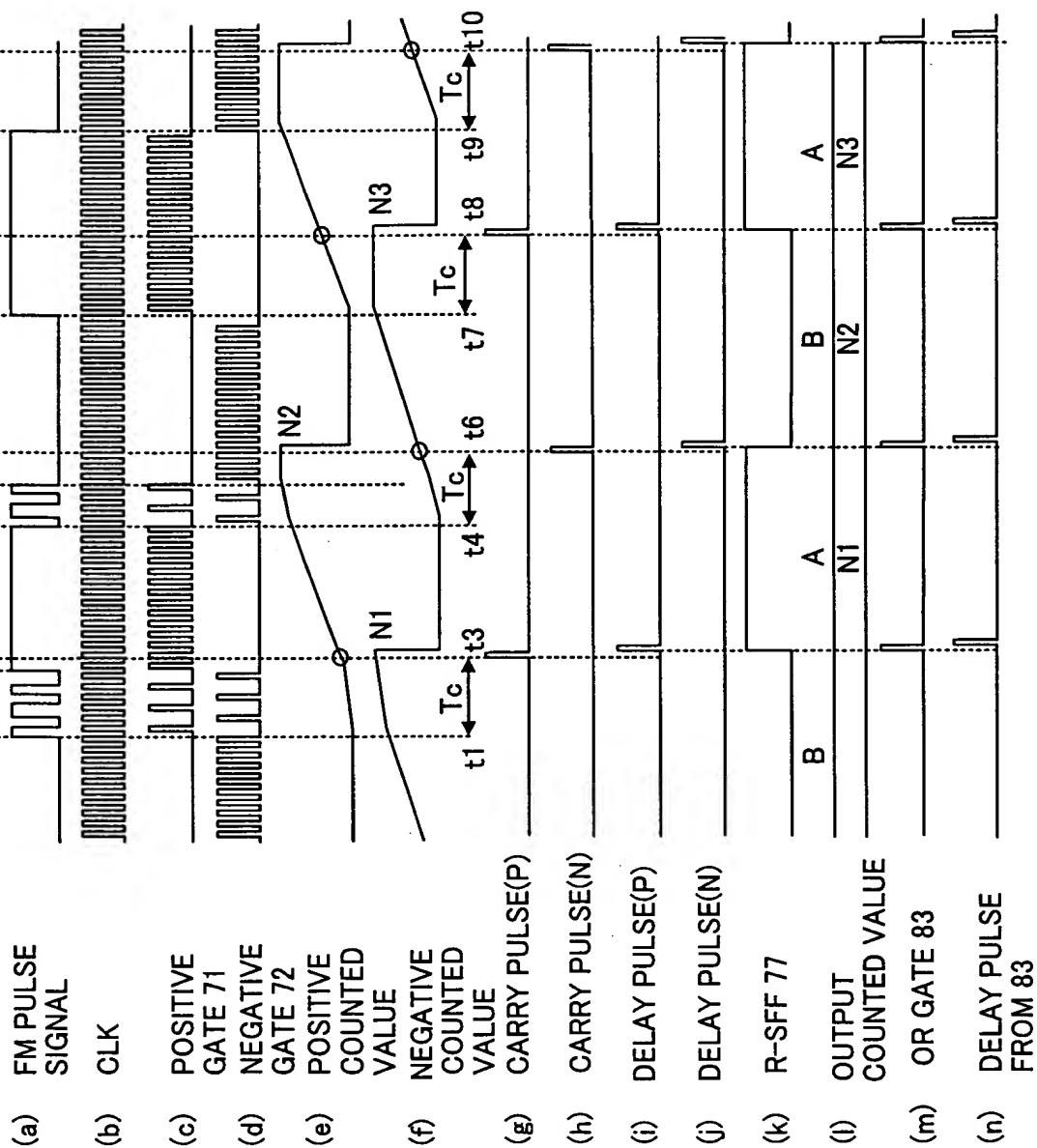
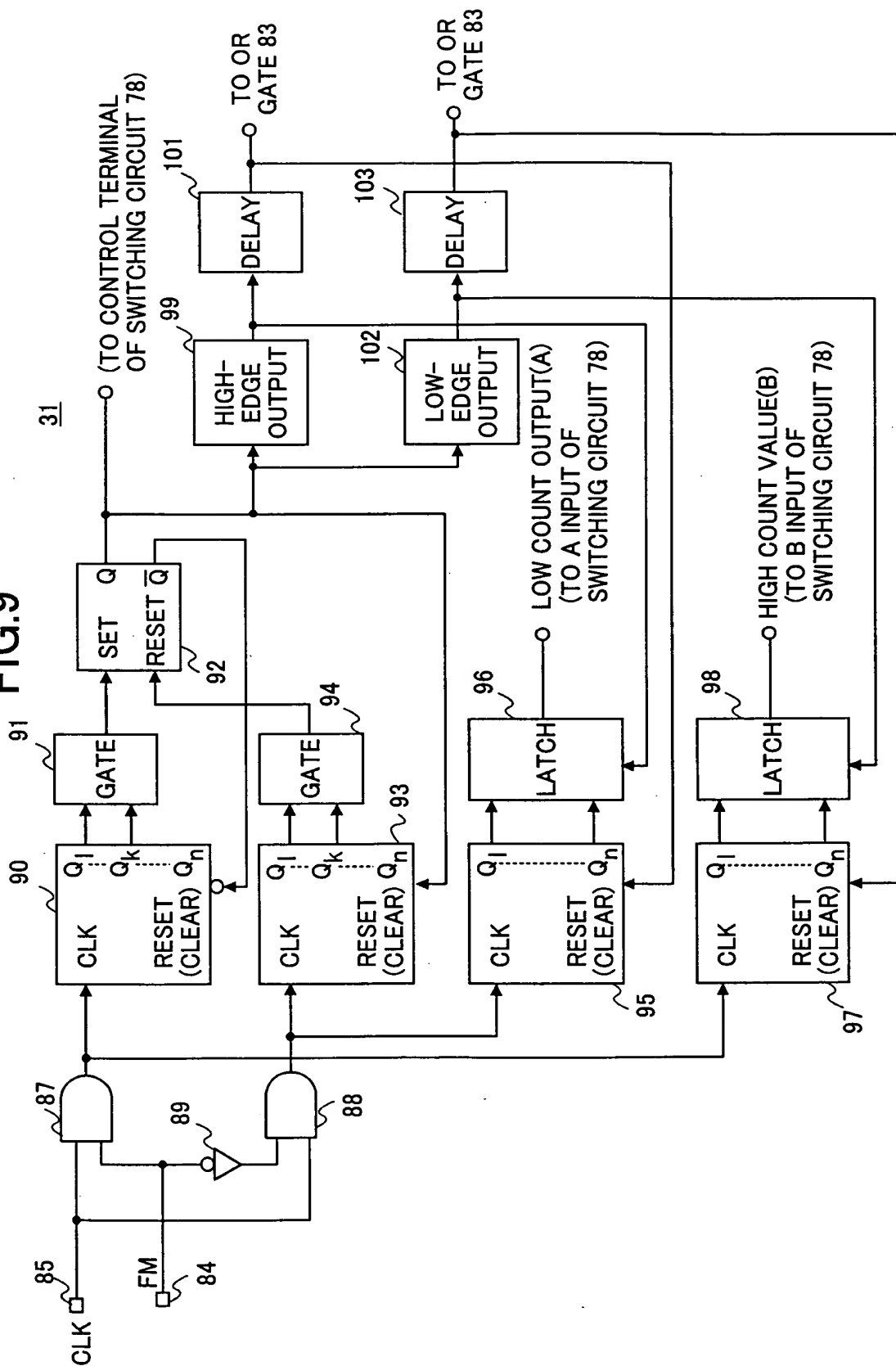


FIG.8

FIG. 9



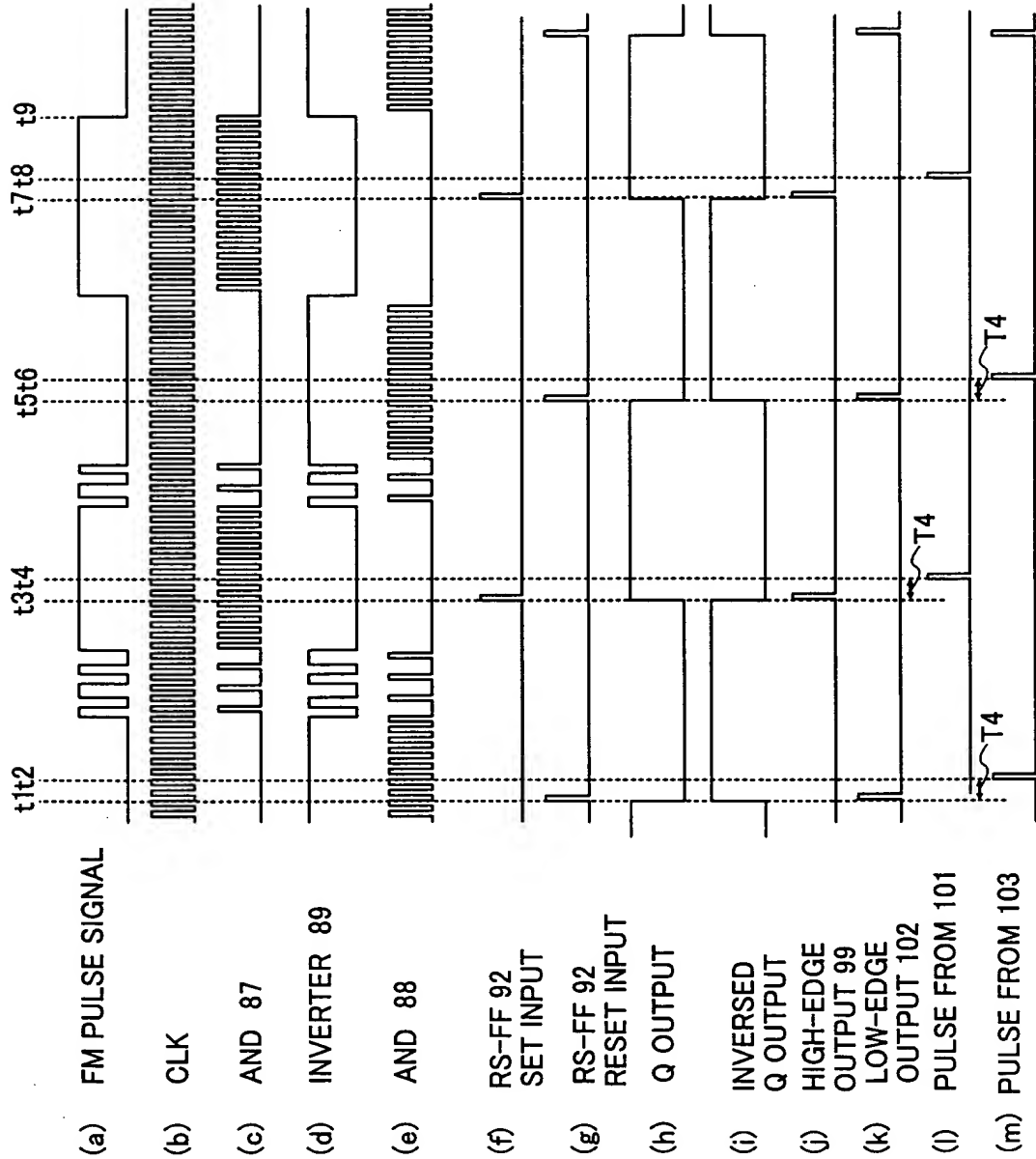
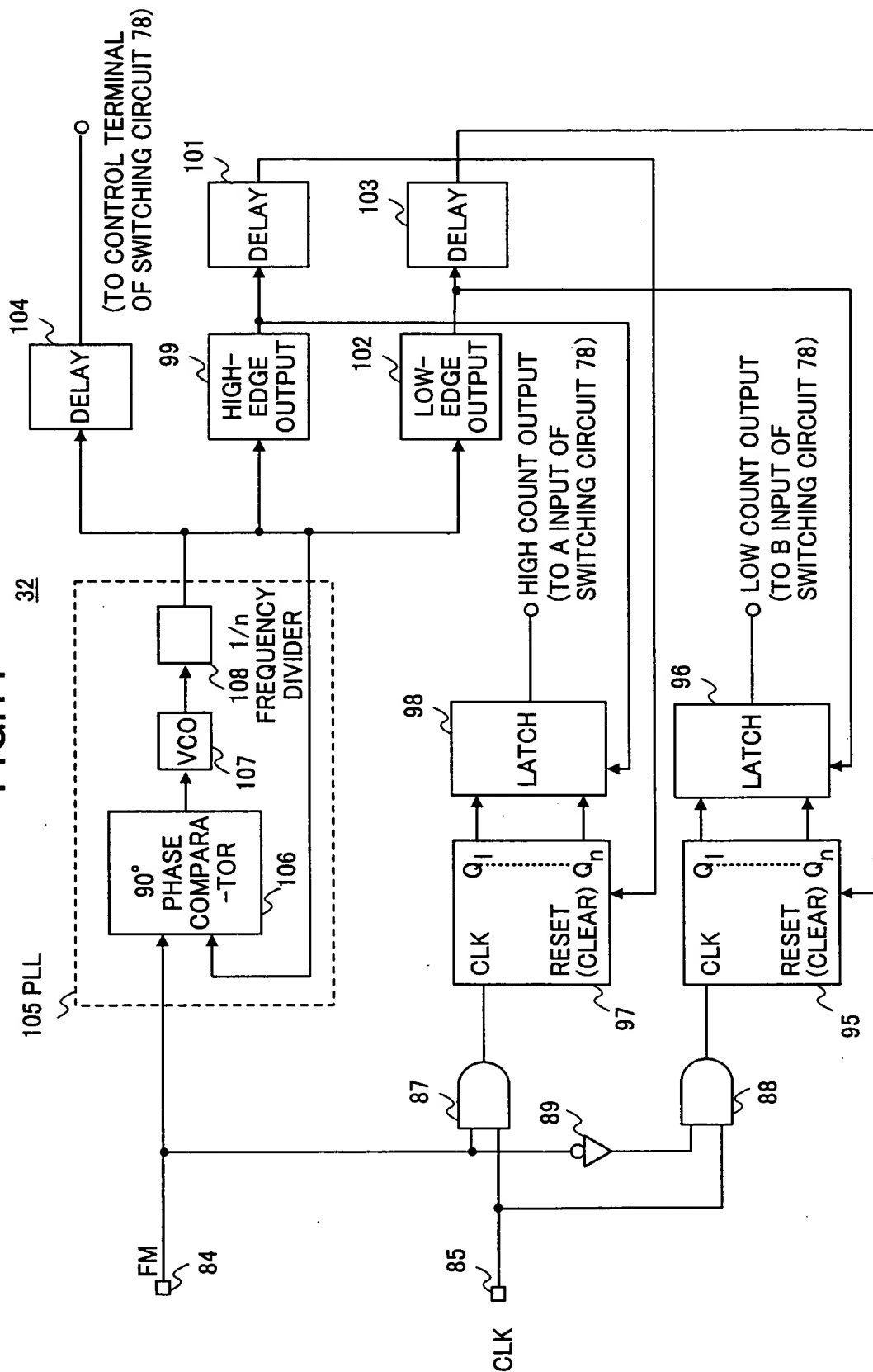


FIG.10

FIG.11



- (a) PLL INPUT (IDEAL)
- (b) PLL OUTPUT
- (c) INPUT SIGNAL (ACTUAL)
- (d) CLK
- (e) AND 87
- (f) INVERTER 89
- (g) AND 88
- (h) HIGH-EDGE OUTPUT 99
- (i) PULSE FROM 101
- (j) LOW-EDGE OUTPUT 102
- (k) PULSE FROM 103
- (l) PULSE FROM 104

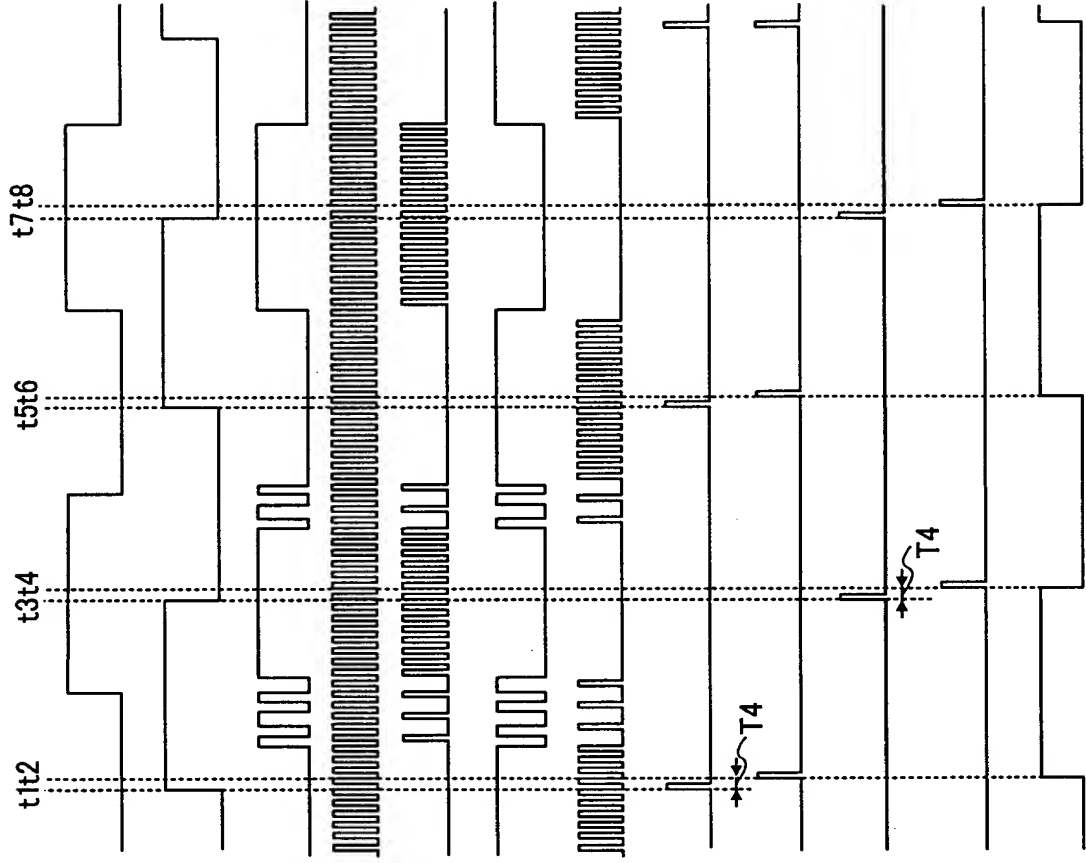


FIG.12